WHAT IS CLAIMED IS:

1. A memory characterization method, comprising the steps:

generating a plurality of tiles forming a memory instance, said plurality of tiles including at least one of a sub-plurality of row decoder tiles, a sub-plurality of input/output (I/O) block tiles, a sub-plurality of bitcell array tiles and at least one control block tile;

providing input and output pins for each tile with respect to a plurality of global signals spanning said memory instance in at least one of a horizontal and a vertical direction;

obtaining a parametric dataset for each of said plurality of tiles; and

creating a hierarchically-stitched parametric netlist for said memory instance by coupling said parametric datasets using said input and output pins of said plurality of tiles with respect to said global signals.

2. The memory characterization method as set forth in claim 1, wherein said tiles are generated based on a minimum area required to encompass an optimal number of memory strap points associated with at least a portion of said global signals.

3. The memory characterization method as set forth in claim 1, wherein said memory instance comprises a post-layout schema, and further wherein said step of obtaining a parametric dataset for each of said plurality of tiles comprises extracting an RC netlist from a select portion of said post-layout schema corresponding to a particular tile.

4. The memory characterization method as set forth in claim 1, wherein said memory instance comprises a pre-layout schema, and further wherein said step of obtaining a parametric dataset for each of said plurality of tiles comprises estimating RC parametric data corresponding to a particular tile based on its wire-delay model.

5. The memory characterization method as set forth in claim 4, wherein said wire-delay model is based on said particular tile's design size parameter.

6. The memory characterization method as set forth in claim 3, wherein said wire-delay model is based on a connection number parameter corresponding to said particular tile.

7. The memory characterization method as set forth in claim 1, wherein said plurality of tiles are generated from a memory instance comprising a read-only memory (ROM) circuit.

8. The memory characterization method as set forth in claim 1, wherein plurality of tiles are generated from a memory instance comprising a static random access memory (SRAM) circuit.

9. The memory characterization method as set forth in claim 1, wherein plurality of tiles are generated from a memory instance comprising a dynamic random access memory (DRAM) circuit.

10. The memory characterization method as set forth in claim 1, wherein said plurality of tiles are generated from a memory instance comprising an electrically programmable ROM (EPROM) circuit.

11. The memory characterization method as set forth in claim 1, wherein said plurality of tiles are generated from a memory instance comprising a flash memory circuit.

12. The memory characterization method as set forth in claim 1, wherein said plurality of tiles are generated from a memory instance comprising a compilable memory circuit.

13. The memory characterization method as set forth in claim 1, wherein said plurality of tiles are generated from a memory instance comprising an embedded memory circuit.

14. The memory characterization method as set forth in claim 1, wherein said plurality of tiles are generated from a memory instance comprising a stand-alone memory circuit.

15. The memory characterization method as set forth in claim 1, wherein said global signals comprise a plurality of pre-decoder signals emanating from said at least one control block tile, said pre-decoder signals being operable to couple said sub-plurality of row decoder tiles in a head-to-tail fashion along said vertical direction.

16. The memory characterization method as set forth in claim 1, wherein said global signals comprise a plurality of wordline signals emanating from said sub-plurality of row decoder tiles.

17. The memory characterization method as set forth in claim 16, wherein each row decoder tile is coupled to a corresponding portion of said plurality of wordline signals, said corresponding portion being operable to couple a select row of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said horizontal direction.

18. The memory characterization method as set forth in claim 1, wherein said global signals comprise a plurality of control signals emanating from said at least one control block tile, said control signals being operable to couple said sub-plurality of I/O block tiles in a head-to-tail fashion along said horizontal direction.

19. The memory characterization method as set forth in claim 1, wherein said global signals comprise a plurality of bitline signals emanating from said sub-plurality of I/O block tiles.

20. The memory characterization method as set forth in claim 19, wherein each I/O block tile is coupled to a corresponding portion of said plurality of bitline signals, said corresponding portion being operable to couple a select column of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said vertical direction.

21. The memory characterization method as set forth in claim 1, wherein said global signals comprise a plurality of power lines coupling said sub-plurality of I/O block tiles with said sub-plurality of bitcell array tiles in said vertical direction.

22. A memory characterization system, comprising:

means for generating a plurality of tiles forming a memory instance, said plurality of tiles including at least one of a sub-plurality of row decoder tiles, a sub-plurality of input/output (I/O) block tiles, a sub-plurality of bitcell array tiles and at least one control block tile;

means for identifying input and output pins for each tile with respect to a plurality of global signals spanning said memory instance in at least one of a horizontal and a vertical direction;

means for obtaining a parametric dataset for each of said plurality of tiles; and

means for creating a hierarchically-stitched parametric netlist for said memory instance by coupling said parametric datasets using said input and output pins of said plurality of tiles with respect to said global signals.

23. The memory characterization system as set forth in claim 22, wherein said means for obtaining a parametric dataset comprises one of a post-layout extractor tool and a pre-layout parametric wire-delay estimator.

24. The memory characterization system as set forth in claim 22, wherein said memory instance comprises one of a DRAM circuit, an SRAM circuit, a ROM circuit, an EPROM circuit and a flash memory circuit.

25. The memory characterization system as set forth in claim 22, wherein said memory instance comprises an embedded memory circuit.

26. The memory characterization system as set forth in claim 22, wherein said memory instance comprises a compilable memory circuit.

27. The memory characterization system as set forth in claim 22, wherein said memory instance comprises a stand-alone memory circuit.

28. The memory characterization system as set forth in claim 22, wherein said global signals comprise a plurality of pre-decoder signals emanating from said at least one control block tile, said pre-decoder signals being operable to couple said sub-plurality of row decoder tiles in a head-to-tail fashion along said vertical direction.

29. The memory characterization system as set forth in claim 22, wherein said global signals comprise a plurality of wordline signals emanating from said sub-plurality of row decoder tiles.

30. The memory characterization system as set forth in claim 29, wherein each row decoder tile is coupled to a corresponding portion of said plurality of wordline signals, said corresponding portion being operable to couple a select row of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said horizontal direction.

31. The memory characterization system as set forth in claim 22, wherein said global signals comprise a plurality of control signals emanating from said at least one control block tile, said control signals being operable to couple said sub-plurality of I/O block tiles in a head-to-tail fashion along said horizontal direction.

32. The memory characterization system as set forth in claim 22, wherein said global signals comprise a plurality of bitline signals emanating from said sub-plurality of I/O block tiles.

33. The memory characterization system as set forth in claim 32, wherein each I/O block tile is coupled to a corresponding portion of said plurality of bitline signals, said corresponding portion being operable to couple a select column of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said vertical direction.

34. The memory characterization system as set forth in claim 22, wherein said global signals comprise a plurality of power lines coupling said sub-plurality of I/O block tiles with said sub-plurality of bitcell array tiles in said vertical direction.

35. A computer-accessible medium operable in connection with a processor environment, said computer-accessible medium carrying a sequence of instructions which, when executed in said processor environment, cause the following steps to be performed:

generating a plurality of repeatable tiles for a memory instance, said plurality of tiles including at least one of a sub-plurality of row decoder tiles, a sub-plurality of input/output (I/O) block tiles, a sub-plurality of bitcell array tiles and at least one control block tile;

identifying input and output pins for each tile with respect to a plurality of global signals spanning said memory instance in at least one of a horizontal and a vertical direction;

obtaining a parametric dataset for each of said plurality of tiles; and

creating a hierarchically-stitched parametric netlist for said memory instance by coupling said parametric datasets using said input and output pins of plurality of tiles with respect to said global signals.

36. The computer-accessible medium as set forth in claim 35, wherein said step of obtaining a parametric dataset for each of said plurality of tiles comprises extracting an RC netlist from a select portion of a post-layout schema corresponding to a particular tile.

37. The computer-accessible medium as set forth in claim 35, wherein said step of obtaining a parametric dataset for each of said plurality of tiles comprises estimating RC parametric data corresponding to a particular tile based on its pre-layout wire-delay model.

38. The computer-accessible medium as set forth in claim 35, wherein said memory instance comprises one of a DRAM circuit, an SRAM circuit, a ROM circuit, an EPROM circuit and a flash memory circuit.

39. The computer-accessible medium as set forth in claim 35, wherein said memory instance comprises an embedded memory circuit.

40. The computer-accessible medium as set forth in claim 35, wherein said memory instance comprises a compilable memory circuit.

41. The computer-accessible medium as set forth in claim 35, wherein said memory instance comprises a stand-alone circuit.

42. The computer-accessible medium as set forth in claim 35, wherein said global signals comprise a plurality of pre-decoder signals emanating from said at least one control block tile, said pre-decoder signals being operable to couple said sub-plurality of row decoder tiles in a head-to-tail fashion along said vertical direction.

43. The computer-accessible medium as set forth in claim 35, wherein said global signals comprise a plurality of wordline signals emanating from said sub-plurality of row decoder tiles.

44. The computer-accessible medium as set forth in claim 43, wherein each row decoder tile is coupled to a corresponding portion of said plurality of wordline signals, said corresponding portion being operable to couple a select row of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said horizontal direction.

45. The computer-accessible medium as set forth in claim 35, wherein said global signals comprise a plurality of control signals emanating from said at least one control block tile, said control signals being operable to couple said sub-plurality of I/O block tiles in a head-to-tail fashion along said horizontal direction.

46. The computer-accessible medium as set forth in claim 35, wherein said global signals comprise a plurality of bitline signals emanating from said sub-plurality of I/O block tiles.

47. The computer-accessible medium as set forth in claim 46, wherein each I/O block tile is coupled to a corresponding portion of said plurality of bitline signals, said corresponding portion being operable to couple a select column of said sub-plurality of bitcell array tiles in a head-to-tail fashion along said vertical direction.

48. The computer-accessible medium as set forth in claim 35, wherein said global signals comprise a plurality of power lines coupling said sub-plurality of I/O block tiles with said sub-plurality of bitcell array tiles in said vertical direction.

49. The computer-accessible medium as set forth in claim 35, wherein said tiles are generated based on a minimum area required to encompass an optimal number of memory strap points associated with at least a portion of said global signals.